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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,931	07/08/2004	Hiroaki Kikuchi	501.43797X00	1570

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/500,931	KIKUCHI ET AL	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 and 2* is/are allowed.

6)☒ Claim(s) *3-9,12 and 13* is/are rejected.

7)☒ Claim(s) *10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 7/08/04. Currently, claims 1-13 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 7/08/04. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3-9, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hori et al., US Patent 6,399,411.

Hori discloses the semiconductor method substantially as claimed. See figures 1-6, and corresponding text, where Hori teaches, pertaining to claim 3, a fabrication method of a semiconductor integrated circuit device, comprising the steps of: (a) forming an insulating film over a substrate (figure 2; col. 7, lines 11-16); (b) after the step (a), inserting the semiconductor substrate into a deposition chamber of a first film forming apparatus (figure 2; col. 7, lines 16-25); (c) adjusting a pressure in the deposition chamber to vacuum or not less than atmospheric pressure (col. 6, lines 17-39); (d) after the step (c), forming a silicon film free of conductive impurity over the insulating film by a chemical film forming method (figure 4; col. 13, lines 50-60); (e) after the step (d) heating the inside of the deposition chamber while adjusting a pressure inside of the deposition chamber to vacuum or not greater than atmospheric pressure (col. 15, lines 15-27); and (f) after step (e), forming a silicon film added with a conductive impurity over the silicon film by a chemical film forming means, wherein a time required for the step (c) is shorter than a time required for the step (e) (col. 15, lines 15-33).

1. Hori teaches, pertaining to claim 4, comprising the steps of: (a) forming an insulating film over a semiconductor substrate (figure 2; col. 7, lines 11-16); (b) after the step (a), forming a silicon film free of conductive impurity over the insulating film by a chemical film forming method by using a second forming apparatus (figure 4; col. 13, lines 50-60); and (c) after the step (b), forming a silicon film added with a conductive impurity over the silicon film by a chemical film forming means by using a first film forming apparatus (col. 15, lines 15-33).

2. Hori teaches, pertaining to claim 5, comprising the steps of: (a) forming an insulating film over s semiconductor substrate (figure 2; col. 7, lines 11-16); (b) after the step (a), inserting

the semiconductor substrate into a deposition chamber of a first film forming apparatus (figure 4; col. 13, lines 50-60); (c) heating the semiconductor substrate while maintaining a pressure in the deposition chamber at atmospheric pressure (col. 6, lines 17-39); (d) after the step (c) , reducing the pressure in a deposition chamber to vacuum or not greater than atmospheric pressure (col. 6, lines 17-39); (e) forming a semiconductor film added with a conductive impurity over the insulating film by a chemical film forming method while maintaining the pressure in the deposition chamber at vacuum or not greater than atmospheric pressure, wherein the step (c), heating is conducted to increase a temperature of the semiconductor substrate upon formation of the semiconductor film or heating is conducted to bring a temperature of the semiconductor substrate close to the first temperature (col. 15, lines 15-33).

3. Hori teaches, pertaining to claim 6, comprising the steps of: (a) forming an insulating film over a semiconductor substrate (figure 2; col. 7, lines 11-16); (b) after the step (a), inserting the semiconductor substrate into a deposition chamber of a first film forming apparatus (figure 2; col. 7, lines 16-25); (c) heating the semiconductor substrate while maintaining a pressure in the deposition chamber at atmospheric pressure (col. 15, lines 15-27); (d) after the step (c) reducing the pressure in the deposition chamber to vacuum or not greater than atmospheric pressure while heating the semiconductor substrate (col. 15, lines 27-30); and (e) forming a semiconductor film added with a conductive impurity over the insulating film by a chemical film forming method while maintaining the pressure in the deposition chamber at vacuum or not greater than atmospheric pressure, wherein a plurality of the semiconductor substrates are disposed in the deposition chamber is a vertical one on which the plurality of the semiconductor substrates are arranged vertically, and in the step (c), heating is conducted to increase a temperature of the

semiconductor substrate to a first temperature of the semiconductor substrate upon formation of the semiconductor film or heating is conducted to bring a temperature of the semiconductor substrate close to the first temperature (col. 15, lines 50-53; col. 16, lines 1-15).

4. Hori teaches, wherein the step (c), a first semiconductor substrate having the lowest temperature among the plurality of the substrates placed in the deposition chamber is heated to the first temperature of the semiconductor substrate upon formation of the semiconductor film or the first semiconductor substrate is heated to bring a temperature thereof close to the first temperature (col. 16, lines 1-15).

5. Hori teaches, pertaining to claim 8, comprising the steps of: (a) forming an insulting film over a semiconductor substrate (figure 2, col. 7, lines 11-16); (b) after the step (a), inserting the semiconductor substrate into a deposition chamber of a first film forming apparatus (figure 2; col. 7, lines 16-25); (c) heating the semiconductor substrate to a first temperature while maintaining the inside of the deposition chamber at first pressure (col. 15, lines 15-27); (d) after the step (c), reducing the pressure in the deposition chamber to be not greater than a second pressure, while heating the semiconductor substrate (col. 15, lines 27-45); and (e) forming, over the insulating film of the semiconductor substrate heated to the first temperature, and silicon added with a conductive impurity by a chemical film forming method while maintaining the pressure inside the deposition chamber at vacuum or a third pressure not greater than atmospheric pressure, wherein in the step (d), pressure is reduced so that the second pressure becomes lower than the third pressure, and wherein the step (c), the first pressure is higher than the third pressure (col. 15, lines 50-53; col. 16, lines 1-15).

6. Hori teaches, pertaining to claim 9, comprising the steps of: (a) forming an insulating film over a semiconductor substrate (figure 2; col. 7, lines 11-16); (b) after the step (a), inserting the semiconductor substrate into a deposition chamber of a first film forming apparatus (figure 2; col. 7, lines 16-25); (c) heating the semiconductor substrate while keeping the inside of the deposition chamber at a first pressure, (d) after the step (c), reducing the pressure in the deposition chamber to be not greater than a second pressure, while heating the semiconductor substrate (col. 15, lines 27-50); and (e) forming a silicon film added with a conductive impurity over the insulating film by a chemical film forming method while keeping the pressure in the deposition chamber at vacuum or third pressure not greater than atmospheric pressure, wherein in the step (d), pressure is reduced so that the second pressure becomes lower than the third pressure, and wherein the step (c), the semiconductor substrate is heated to bring a temperature thereof close to the first temperature while maintaining the first pressure to be higher than the third pressure (col. 15, lines 50-53; col. 16, lines 1-30).

7. Hori teaches, pertaining to claim 12, wherein a plurality of the semiconductor substrates are disposed in the deposition chamber is a vertical one on which the plurality of the semiconductor substrates are arranged vertically, and in the step (c), heating is conducted to increase a temperature of the semiconductor substrate to a first temperature of the semiconductor substrate upon formation of the semiconductor film or heating is conducted to bring a temperature of the semiconductor substrate close to the first temperature (col. 15, lines 50-53; col. 16, lines 1-15).

8. Hori teaches, pertaining 13, wherein the first pressure is atmospheric pressure (col. 6, lines 17-40).

9. It would have been obvious to one of ordinary skill in the art to incorporate, adjusting the pressures with regards to atmospheric pressure or vacuum, the temperature, etc.. with the motivation of creating a desired film forming process, which would result in routine experimentation.

Allowable Subject Matter

10. Claims 10 and 11 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

12. The closest prior art of record, Hori et al., US Patent 6,399,411, fails to show the following steps:

13. pertaining to claim 10, "wherein a time required for the step (c) is longer than required for step (d)"

14. Pertaining to claim 11, "wherein the time required for the step (c) is 0.1 times or greater but not greater than 13 times as long as the time required for the step (d)."

15. Claims 1 and 2 are allowed over prior art of record.

16. The following is an examiner's statement of reasons for allowance:

17. The closest prior art of record, Hori et al., US Patent 6,399,411, fails to show the following steps:

18. pertaining to independent claim 1, "wherein a time required for the step (c) is longer than required for step (d)"

19. Pertaining to independent claim 2, "wherein the time required for the step (c) is 0.1 times or greater but not greater than 13 times as long as the time required for the step (d)."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
March 20, 2006

MICHAEL LEBENTRITT
SUPERV SORY PATENT EXAMINER